REMARKS

The application has been reviewed in light of the Final Office Action mailed June 18, 2004. At the time of the Final Office Action, claims 1-9, 11-40, 42-52 and 55-66 were pending in this application, and all of these claims were rejected.

I. Brief Summary of the Invention

Writing voltage values to columns of a liquid crystal display (LCD) requires a voltage source(s) capable of rapidly charging a capacitor. When using a voltage source, the final voltage value on a column is approached exponentially in time, this time is typically from about 5 to 30 nanoseconds. The voltage source amplifier(s) used to charge the column capacitance require a large quiescent operating current in order to achieve the 5 to 30 nanosecond charge time. The amount of current eventually diverted over to the LCD pixel capacitance during voltage charging thereof is infinitesimal compared to the voltage source amplifier quiescent operating current. Thus a significant amount of power is wasted in the LCD driver electronics which reduces the feasibility of using an LCD in applications requiring very low power.

The present invention overcomes the above-identified problem and deficiency of existing LCD driver technologies by providing a system and method for quickly and accurately writing video frame information to a matrix of pixels of a liquid crystal display (LCD) using a minimum amount of power. The present invention charges the capacitance of each column to a desired voltage by using a current source. When using the current source, the voltage being charged onto the column capacitance increases linearly with the constant current from the current source being sent thereto and is very fast (linear, not exponential). The LCD wastes no power

for quiescent current of the driving electronics (no voltage source is needed). All prior art LCD voltage source column charging circuits suffer from excessive power usage.

The present invention uses a constant current source to create current pulses having controlled constant amplitudes and pulse-widths for charging columns of a liquid crystal display to voltages representative of pixel gray scale shades. A single constant amplitude and width controlled current pulse is used per video frame to charge a column capacitance to a desired gray scale voltage for transfer of that gray scale voltage to a respective liquid crystal pixel capacitor. The current source constant amplitude and pulse-width are both controlled in combination to achieve very high resolution of the resulting linear, low power, voltage charge on the column capacitance. The current pulse characteristics (constant amplitude and pulse-width) may be stored in a gamma lookup table (LUT) so that the desired current pulse constant amplitude and pulse-width for each of the desired gray scale shades of the liquid crystal display (LCD) may be selected as required by the received pixel image to be displayed on the LCD. By selectively controlling both the constant amplitude current and the pulse-width, much finer resolution (granularity) of the resultant column voltages may be obtained. The resolution may be the number of bits applied to the current source digital-to-analog converter (IDAC) for a constant amplitude current from the IDAC, represented by A, and the pulse-width time duration of the constant amplitude current from the IDAC, represented by T. The resolution (granularity) of the resulting current pulse used to charge the column capacitance to a desired voltage will be A x T. Thus, the voltage charge to the column is not limited to the resolution of the IDAC, and may have a much greater resolution than is possible with only the bit resolution of the IDAC.

II. Rejections under 35 U.S.C. § 103(a)

Applicant respectfully traverses the following rejections and submits that the references relied upon for rejection of the claims do not teach or suggest, individually or in combination, what is being claimed in independent claims 1, 37 and 49.

A. Claims 1, 7-9, 11, 12, 25, 26, 31-34, 37-40, 42, 43, 46-52, 55-59, and 64 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,496,173 issued to Albu et al., (hereinafter "Albu") in view of U.S. Patent No. 6,094,243 issued to Norio Yasunishi (hereinafter "Yasunishi").

The Albu patent discloses a counter (12) that controls a lookup table (LUT) (32) that is used to control a current source digital-to-analog converter (IDAC) (34). The IDAC (34) input coupled to the LUT (32) has a stair step/ramping binary value that is counting up *i.e.*, increasing. This ramping input produces a plurality of linear constant current source values increasing over time (see Figure 3 of Albu). The Albu invention teaches using a plurality of ramping current values (increasing stair step) within a single video frame time for reducing noise in the LCD display. The plurality of ramping current values charge the pixel column capacitance to various voltage values depending upon how long a column is connected to the output of the IDAC (34). There is no control of how the column capacitance is charged to a desired voltage other than the length of time the column capacitance is coupled to the IDAC (34).

The output of the IDAC (34) is initially coupled to all of the LCD pixel columns (28) through current amplifier/switches (36, 38). Each of the column switches 38 has an associated comparator (24) that monitors the output of the counter (12) and predetermined counter values for each column (28) that are stored in a data buffer (22). When the digital value of the counter (12) matches a predetermined counter value for a column voltage charge, the comparator (24) will turn off the respective column switch (38), thereby stopping any further

voltage charging of that column (28) from the stair step plurality of current values. In effect each column stays connected to the voltage charging circuit (34, 18, 36) until a desired voltage value, *i.e.*, what is stored for that column 28 in the data buffer (22). As each voltage value for a column (28) is reached, as determined by the digital comparator (24), that column is disconnected from the voltage charging circuit (34, 18, 36). This operation is like a bus dropping passengers off along a well defined route (each column gets off the voltage charging bus when it reaches its desired voltage value). *See generally*, Albu, column 3, lines 11-44. The resolution accuracy of the voltage charging current source of Albu can only be the absolute resolution of the IDAC since the current charging steps must equal the IDAC digital input resolution.

Albu does not address or take into account the change in capacitance that results from a column being disconnected from the charging circuit. The current charging disclosed in Albu simply ramps up based upon the value of the counter (12), thus changes in connected column capacitance will greatly alter the accuracy of a voltage charge into a capacitance from a current source since voltage is dependent upon the amount of charge (current) injected into the capacitance in combination with the capacitance value. Significant errors may be introduced by changing the capacitance values while trying to charge column(s) from a current source. Also the voltage charging method disclosed in Albu has only the resolution of the IDAC (34) since pulse-width is not controlled, only the time in which a column is connected to the charging source, IDAC (34).

Yasunishi teaches dividing a video frame into subframes such that the gray scales of pixels may be changed for each subframe and the average of the subframe gray scales determine the resultant gray scale for the frame. The Yasunishi reference states:

> The device includes: a display data transformer for receiving input image data for one frame, for dividing a selection period for each row electrode in the frame into subframes of a number equal to or greater than a number of gray-scale bits representing a gray-scale level of the input image data, the scanning signal being applied to the row electrode during the corresponding selection period, and for generating binary display data in which respective binary data is associated with each subframe according to the gray-scale bits; a pulse width controller for controlling the division of the selection period in the display data transformer and for setting a respective subframe period independently for each subframe; and a pulse amplitude controller for transforming the binary display data by setting a respective voltage amplitude independently for each subframe according to the binary display data so as to generate a display signal having a respective voltage value set independently for each subframe. Thus, an effective voltage according to the gray-scale bits of the input image data is applied to the liquid crystal display layer so as to conduct a gray-scale display for the input image data.

Yasunishi at column 3, lines 21-41.

Thus Yasunishi merely discloses applying various voltage values to the LCD pixel display irrespective of the amount of current used to charge the pixel capacitors. This reference teaches the prior art method of controlling gray scale voltages of the LCD pixels. Use of subframe averaging of various gray scale values taught by Yasunishi is not similar to what is claimed in the present invention of using a constant amplitude current pulse having a well defined pulse-width for charging a column capacitance. The pulse width control circuit (21) of Yasunishi is used for setting a period independently for each subframe for assertion of a gray scale voltage to charge a column capacitance. See Column 12, lines 1-17 of Yasunishi.

The exact pulse width of the voltage charging circuit is immaterial in Yasunishi because when using a standard voltage source, as disclosed in Yasunishi, the column capacitance will charge to that voltage irrespective of time since current is not limited in any way when using a voltage source as is well known to those of ordinary skill in the prior art liquid crystal displays.

Yasunishi also does not teach or suggest using a constant amplitude current source having a defined pulse width to controllably charge a column capacitance so as to minimize the amount of current surge (noise) generated by the voltage charging operation. A great deal of power is expended when charging column capacitances with a corresponding amount of circuit noise. The present invention overcomes these inherent problems with the technology taught by Yasunishi. Also the time slots used for the subframes in Yasunishi do not suggest what control of the pulse width accomplishes in the present invention.

Applicant respectfully submits that the Yasunishi reference does not teach or suggest the new, novel and non-obvious advantages achieved in using the present invention of reducing power consumption by charging a column capacitance with a constant amplitude current source being applied over an exact length of time (*i.e.*, controlled pulse-width). In the present invention, the voltage resulting on the column capacitance is strictly dependent upon the value of the constant amplitude current source applied to the column capacitance over the defined time (pulse width) for a frame of video. This is not taught or suggested in the Yasunishi reference since this reference uses a voltage source (prior art) and the pulse widths reference in this reference relate to subframe time intervals of various gray scales that are averaged together to achieve finer granularity gray scales of the LCD.

Neither Albu nor Yasunishi teach or suggest, individually or in combination, controlling the pulse-width of a constant amplitude current charging pulse for enhanced gray scale resolution. This, in contrast to what is disclosed in either Albu or Yasunishi, the present invention injects a single unique current pulse, having a constant current amplitude and pulse-width, for each individual LCD column per frame of video. Thus the present invention takes advantage of the greater resolution of combining both a constant current amplitude and pulse-

width time duration to more finely control the amount of current charge injected into each individual column capacitance than is possible with the references relied upon. This results in many more gray scale shades available even with a relatively low input resolution DAC.

Claims 7-9, 11, 12, 25, 26, 31-34 and 64 depend from independent Claim 1 and contain all limitations thereof. Claims 38-40, 42 and 46-52 depend from independent Claim 37 and contain all limitations thereof. Claims 50-52 and 55-59 depend from independent Claim 49 and contain all limitations thereof.

B. Claims 1, 7-9, 11, 12, 25, 26, 31-34, 37-40, 42, 43, 46-52, 55-59 and 64 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of U.S. Patent No. 5,103,112 issued to George R. Briggs (hereinafter "Briggs").

Briggs teaches a simple, low cost binary value controlled voltage source gates that may be implemented on an amorphous silicon substrate in great number due to the low cost and simplicity of the circuit. The Briggs invention is compared and contrasted with a programmable counter which is typically used for timing the on state of a gate ("width of the pulse") which allows a ramping voltage to pass through to charge an LCD element, *e.g.*, LCD column. As stated in Briggs:

> Display information represented by binary numbers are converted into variable width pulses which pulses are used to control conduction times of switching transistors. A ramp voltage is applied to one electrode of the switching transistor, the other electrode being coupled to a display element. The transistor is conditioned to conduct at predetermined intervals and is turned off as a function of the variable width pulse. At the time the transistor is turned off, the ramp voltage, and thus the potential applied to the display element is proportional to the binary value controlling the pulse-width.

Briggs, column 1, lines 20-31.

Briggs teaches charging a LCD element, *e.g.*, column, with a ramping voltage source until the ramping voltage source reaches a desired voltage value, then the ramping voltage source is disconnected from the LCD column. Briggs does not teach or suggest using a current source having a "controlled amplitude and pulse-width" for charging a LCD column. The present invention uses a controlled current amplitude of constant value which is coupled to the LCD column for a controlled duration of time (pulse-width). The product of the controlled constant amplitude and controlled duration of time results in a much better resolution (granularity) then what is possible with what is taught in the references relied upon.

Briggs teaches using a voltage ramp generator that is connected to an LCD element until the voltage ramp generator output has reached the desired voltage value on the LCD element. Albu also teaches using a counter (12) to drive the input of the IDAC (34). This counter input also results in the output (current) of the IDAC (34) ramping up while charging the LCD column until a value of the counter (12) is reached that matches the desired charging current value. The resolution of Albu is only that of the number of binary input bits of the IDAC (34). Albu does not teach or suggest using a controlled current amplitude of constant value which is coupled to the LCD column for a controlled duration of time (pulse-width), as claimed in the present invention.

No motivation is found in either of the references to combine a constant amplitude current source with a controlled pulse-width since Briggs only teaches a ***ramping*** voltage source coupled to an LCD element and controlled by a certain desired pulse-width. Albu only teaches a ***ramping*** current source controlled by a count value (input to the IDAC) being reached then the current source is de-coupled from the LCD column being charged. Neither of the references, individually or in combination, teach or suggest the new, novel and non-obvious

feature of the present invention which is controlling both the amplitude of a constant current source and the pulse-width (time duration) of that constant amplitude current source to uniquely charge each of the respective columns of an LCD, as claimed in independent claims 1, 37 and 49.

Claims 7-9, 11, 12, 25, 26, 31-34 and 64 depend from independent Claim 1 and contain all limitations thereof. Claims 38-40, 42 and 46-52 depend from independent Claim 37 and contain all limitations thereof. Claims 50-52 and 55-59 depend from independent Claim 49 and contain all limitations thereof.

C. Claims 2-4, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or over Yasunishi as applied to Claim 1 above, and further in view of U.S. Patent No. 6,459,395 issued to Kida et al. (hereafter "Kida").

Kida merely teaches column and row selection in a LCD. The references relied upon do not teach or suggest, individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge, at a very fine resolution, each of the respective columns of an LCD, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 2-4, 27 and 28 depend from independent Claim 1 and contain all limitations thereof.

D. Claims 5, 6, 29, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi and Kida as applied to Claim 2 above, and further in view of U.S. Patent No. 6,067,083 issued to Glen et al. (hereinafter "Glen").

Glen teaches saving power by turning off a video graphics processor during horizontal and vertical retrace times in an analog cathode ray tube (CRT) video display. Glen also teaches a look-up table DAC for use with the CRT display. There is no teaching or suggestion to apply the Glen invention to an LCD (LCD is digitally controlled, not analog and

does not require horizontal and vertical retrace times). Kida merely teaches column and row selection in a LCD. None of the references relied upon teach or suggest, individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 5, 6, 29 and 30 depend from independent Claim 1 and contain all limitations thereof.

E. Claims 13, 14, 44, and 45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi as applied to Claims 1 and 37 above, and further in view of U.S. Patent No. 5,970,106 issued to Masanori Izumikawa (hereinafter "Izumikawa").

Izumikawa teaches a phase-locked-loop (PLL) clock system. There is no teaching nor suggestion to use the Izumikawa invention in a LCD to control a current pulse amplitude and pulse-width for charging a LCD column voltage. Likewise there is no suggestion to combine the PLL of Izumikawa with the other references relied upon to control the amplitude and pulse-width of a current source used to charge individual LCD columns to specific voltage levels, nor do the references relied upon teach or suggest the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 13 and 14 depend from independent Claim 1 and contain all limitations thereof. Claims 44 and 45 depend from independent Claim 37 and contain all limitations thereof.

F. Claims 15-18 and 35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi as applied to Claim 1 above, and further in view of U.S. Patent No. 5,453,991 issued to Suzuki et al. (hereinafter "Suzuki").

Suzuki teaches internal integrated circuit inspection circuitry that is directed to wafer-level inspection. There is no relationship to LCD column voltage charging, nor is there any motivation to combine Suzuki with the other references relied upon to teach or suggest controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD to specific voltage levels, as discussed above. Nor do the references relied upon teach or suggest the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 15-18 and 35 depend from independent Claim 1 and contain all limitations thereof.

G. Claims 19-21, and 60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi as applied to Claim 1 or 49 above, and further in view of U.S. Patent No. 5,668,650 issued to Mori et al. (hereinafter "Mori").

Mori teaches an internal amorphous thin film transistor (TFT) structure that internally compensates for the gate-source capacitance Cgs of each TFT. None of the references relied upon teach or suggest, either individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD, as discussed above, to specific voltage levels or the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 19-21 depend from independent Claim 1 and contain all limitations thereof. Claim 60 depends from independent Claim 49 and contains all limitations thereof.

H. Claims 22, 23, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi and Mori as applied to Claims 19-21 above, and further in view of U.S. Patent No. 6,081,250 issued to Shimada et al. (hereinafter "Shimada").

Shimada teaches a method to reduce the effect of column and row delay times by doubling the number of columns and rows, and modifying the signals used in them. This method is not relevant nor required for the present invention. None of the references relied upon teach or suggest, either individually or in combination, what is being claimed, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 22, 23 and 36 depend from independent Claim 1 and contain all limitations thereof.

I. Claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi and Mori as applied to Claims 19-21 above, and further in view of U.S. Patent No. 3,538,450 issued to Andrea et al. (hereinafter "Andrea").

Andrea teaches using a varactor capacitor to electronically control the frequency of an oscillator. There is no teaching nor suggestion in Andrea for what is being claimed. None of the references relied upon teach or suggest, either individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD to specific voltage levels or the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claim 24 depends from independent Claim 1 and contains all limitations thereof.

J. Claims 61-63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi as applied to Claim 1 above, and further in view of U.S. Patent No. 5,940,057 issued to Lien et al. (hereinafter "Lien").

Lien teaches solving crosstalk in amorphous silicon TFT displays be line inversions and pre-charging of the display electronics. This is not required nor desired in the present invention. There is no suggestion to combine Lien with the other references relied upon to teach or suggest, either individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD to specific voltage levels or the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claims 61-63 depend from independent Claim 1 and contain all limitations thereof.

K. Claims 65 and 66 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Albu in view of Briggs or Yasunishi and Mori as applied to Claim 19 and 20 or as applied to Claim 60 above, and further in view of U.S. Patent No. 6,151,238 issued to Smit et al. (hereinafter "Smit").

Smit teaches using flusable links to adjust capacitance. However, Smit in combination with the other references relied upon do not teach or suggest, either individually or in combination, controlling both constant amplitude current pulses and pulse-widths thereof to uniquely charge each of the respective columns of an LCD to charge individual LCD columns to specific voltage levels or the high resolution gray scale shade selection possible when using the present invention, as discussed above regarding Albu, Yasunishi and Briggs.

Claim 65 depends from independent Claim 1 and contains all limitations thereof. Claim 66 depends from independent Claim 49 and contains all limitations thereof.

L. Examiner's Response to Prior Arguments

Ito et al., U.S. Patent No. 5,877,738 (Ito) teaches applying a voltage source to charge column capacitance of an LCD. The Ito reference suffers from the same short comings of all prior art voltage source column capacitance driver circuits. The statement made in column 31, lines 58-65 of Ito is not entirely correct in that voltage and current are being confused in the statements made about when charging a column capacitance with a high voltage for a short time or a low voltage for a long time. Voltage transfer between a voltage source and a capacitance is a function of the series connected resistance therebetween. The voltage on the capacitor is determined by the RC time constant of:

$$V(t) = E\,(1-e^{-t/RC})$$

Thus the charging current into the column capacitance is a function of the series resistance between the voltage source and the column capacitance. Current from a voltage source into a discharged capacitor is a function of the series connected resistance therebetween (a voltage source is assumed to have infinite current availability, not so in actual practice). Therefore, the series resistance must be know before any quantitative assessment of what resulting voltage level on a column capacitance will be during connection to a voltage source for a given time period. Thus Ito has mischaracterized the relationship of voltage, resistance and application time in determining the amount of energy stored on a column capacitance. Since the lower the resistance, the faster will be the charging of the capacitance at an exponential rate.

Ito merely teaches prior art charging of column capacitance by a voltage source without regard to the new, novel and non-obvious features and advantages inherent in the present invention of controlling the actual voltage on a column capacitance with a precision, high resolution constant amplitude and pulse-width current pulse generated from a current source, not

from a voltage source. By using a constant current source whose current amplitude may be controlled at a constant current value, the present invention charges the column capacitance at a ***linear rate*** (not exponential) that may easily be further controlled over a given time period for a precision desired voltage on the column. Series resistance is not a substantial factor when using the present invention. None of the references relied upon, either individually or in combination, teach or suggest what is being claimed in the present invention, as discussed above.

III. Arguments Relating to the Combination of the References Asserted

A. No Basis or Support Has Been Shown in the Rejection of the Claims That One Having Ordinary Skill in the Art at the Time of the Invention Would Be Motivated to Modify the References Relied Upon to Produce the Invention

Throughout the rejections the assert of "it would have been obvious to one of ordinary sill in the art at the time the invention to combine" the various elements found in the references relied upon to produce the present invention is respectfully traversed. It is improper to use the invention disclosed as a template to pick and choose from the various references without some teaching or motivation found in these references to combine the elements necessary to produce the claimed invention.

Pursuant to MPEP § 2144.03, incorporated by reference herein for all purposes, Applicant respectfully submits that no prior art reference documents have been disclosed nor asserted that would substantiate that one having ordinary skill in the art at the time of the invention would be motivated to modify the references relied upon to produce the present invention. One cannot convert charging a column capacitance with a voltage source just because there is a reference to a pulse width control, nor can one convert a ramping or stair step current source driven by a counting circuit to produce a constant amplitude current source applied over a specific time (pulse-width) to charge a column capacitance to a desired gray scale voltage,

without some teaching or suggestion found in the references relied upon to do so.

"When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness." *In re Lee*, 61 U.S.P.Q.2d 1430, 1433 (Fed. Cir. 2002), citing *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 U.S.P.Q.2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the Graham factors).

Moreover, the Federal Circuit in *In re Lee* further indicated that:

> "The factual inquiry whether to combine references must be thorough and searching." *Id.*, 61 USPQ2d at 1433. "It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with." *Id.*, citing, *Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'") (quoting *C.R. Bard, Inc., v. M3 Systems, Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) ("'teachings of references can be combined only if there is some suggestion or incentive to do so.'") (emphasis in original) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).
>
> "The need for specificity pervades this authority." *In re Lee*, 61 USPQ2d at 1433, 1434, citing *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of

> the claimed invention, would have selected these components for combination in the manner claimed"); *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); *In re Fritch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

Finally, the Federal Circuit noted that:

> "This factual question of motivation is material to patentability, and could not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *In re Lee*, 61 USPQ2d at 1434, quoting *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983).

Applicant respectfully submits that the obligation required for a *prima facie* determination of obviousness under the holding in *In re Lee* has not been met. None of the references relied upon teach or suggest the problem and/or solution of the problem as disclosed and claimed in the present invention. Therefore, someone skilled in the art would not be prompted to combine these documents. "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." *In re Napier*, 55 F.3d 610, 613, 34 USPQ 1782, 1784 (Fed. Cir. 1995), quoting *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (additional citations omitted).

B. The Invention Itself Cannot Be Used as a Template to Pick and Choose Elements from Prior Art References

Applicant respectfully submits that alleged identification in the prior art of each individual element claimed is insufficient to defeat patentability of the claimed invention as a whole. *In re Kotzab*, 217 F.2d 1365, 1369, 55 U.S.P.Q.2d 1313, 1316 (Fed. Cir. 2000). Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *Id.* None of the references relied upon make any suggestion of the problem or solution for the problem disclosed and solved by the present invention.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicant reserves the right to subsequently take up prosecution on the claims as originally filed in this or appropriate continuation, continuation-in-part and/or divisional applications.

Applicant respectfully requests that the amendments submitted herein be entered, and further requests reconsideration in light of the amendments and remarks contained herein.

Applicant respectfully requests withdrawal of all objections and rejections, and that there be an early notice of allowance.

SUMMARY

In light of the above amendments and remarks, Applicant respectfully submits that the application is now in condition for allowance and early notice of the same is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone, facsimile or electronic mail, as indicated below.

Applicant believes that there are no fees due in association with the filing of this Response. However, should the Commissioner deem that any fees are due, including any fees for any extensions of time, Applicant respectfully requests that the Commissioner accept this as a Petition therefor, and directs that any fees be debited from Baker Botts L.L.P. Deposit Account No. 02-0383, Order Number 075115.0109.

Respectfully Submitted,
BAKER BOTTS L.L.P. (023640)

By: Paul N. Katz

Paul N. Katz
Reg. No. 35,917
One Shell Plaza
910 Louisiana Street
Houston, Texas 77002-4995
Telephone: 713.229.1343
Facsimile: 713.229.7743
E-Mail: Paul.Katz@bakerbotts.com
ATTORNEY FOR APPLICANT

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